REMARKS

The Office Action dated October 17, 2005, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 2-4, 6-9, 11-13, 15-27, 29-31, 33-36, 38-40, 42-54, 56-58, 60-63, 65-67 and 69-81 have been withdrawn from consideration. Claims 1, 5, 10, 14, 28, 32, 37, 41, 55, 59, 64 and 68 are pending in the present application for examination and are respectfully submitted for consideration.

Rejection of Claims 1, 10, 28 and 37 under 35 U.S.C. § 102(b)

Claims 1, 10, 28 and 37 were rejected under 35 U.S.C. § 102(b) as being anticipated by Early et al. (U.S. Patent No. 5,391,999, hereinafter "Early"). The Applicants respectfully traverse the rejection.

In making the rejection, the Office Action characterized Early as allegedly disclosing "a buffer circuit (47) buffering an output of said sampling circuit; ... and a buffer control circuit (45, 46, 50 and 51) keeping a small input signal dependency of the output of said buffer circuit until (col. 10, lines 35-45) carrying out said sampling (fig. 5; col. 10, lines 4-15; col. 10, lines 44-53, **54-58**)."

The Applicants respectfully disagree with the Office Action's characterization of Early and submit that element 47 of Early is neither comparable nor analogous to the buffer circuit of the present invention. For example, it is submitted that the input voltages of the buffer circuit 320 of the present invention are not caused by a charge-sharing operation as applied in Early. It is further submitted that elements 45, 46, 50 and 51, taken alone or in combination, are neither comparable to the buffer control circuit of the present invention.

For example, it is submitted that Early discloses switched-capacitors (glitchless switched-capacitor biquad low pass filter), and transistors controlled by clock signals Φ1 and Φ2 are generally used in the switched-capacitors. A illustrated in Fig. 2 of Early, input voltages of an operational amplifier 47 are specified by sharing capacitors 44, 52 and capacitors 49, 53. It is submitted that the capacitors 44 and 49 are disposed between transmission gates 43 and 48 and the operational amplifier 47, respectively.

In contrast, the present inventions as recited in claims 1, 10, 28 and 37 are directed to a buffer circuit for buffering an output of the sampling circuit, and a buffer control circuit for keeping a small input signal dependency of an output of the buffer circuit until carrying out the sampling of an input signal. In other words, the Applicants submit that Early fails to disclose or suggest at least the following features recited in the following claims.

> Claim 1:
> a buffer circuit buffering an output of said sampling circuit;
> ...
> buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling
>
> Claim 10:
> a buffer circuit buffering an output of said sampling circuit;
> ...
> a buffer control circuit keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling.
>
> Claim 28:
> a buffer circuit buffering an output of said sampling circuit;
> ...

a buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling.

Claim 37:

a buffer circuit buffering an output of said sampling circuit;

...

a buffer control circuit keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling.

Therefore, the Applicants submit that in order to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Early clearly fails to disclose or suggest each and every feature of claims 1, 10, 28 and 37. Accordingly, the Applicants respectfully submit that claims 1, 10, 28 and 37 are not anticipated by the disclosure of Early. Therefore, the Applicants respectfully submit that claims 1, 10, 28 and 37 are allowable.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Rejection of Claims 5, 14, 32, 41, 55, 59, 64 and 68 under 35 U.S.C. § 103(a)

Claims 5, 14, 32, 41, 55, 59, 64 and 68 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawabata (U.S. Patent No. 6,452,518) in view of Early. The Applicants respectfully traverse the rejection.

Early is discussed above, the Applicant has clearly established that Early fails to disclose or suggest at least the features of: a buffer circuit buffering an output of said sampling circuit; a buffer control circuit keeping a small input signal dependency of the output of said buffer circuit until carrying out said sampling; and a buffer control circuit

keeping a substantially constant value of the output of said buffer circuit until carrying out said sampling, as recited in claims 55 and 64, respectively.

Kawabata merely relates to an A/D converter and a calibration unit incorporated in a semiconductor device testing apparatus, and only discloses a bit interleaving apparatus.

In view of the above, the Applicants submit that Kawabata in view of Early fail to disclose or suggest each and every element recited in claims 5, 14, 32, 41, 55, 59, 64 and 68 of the present application.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, the Applicants respectfully submit that each of claims 1, 5, 10, 14, 28, 32, 37, 41, 55, 59, 64 and 68 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully request that claims 1, 5, 10, 14, 28, 32, 37, 41, 55, 59, 64 and 68 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together

with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 100021-00066.**

Respectfully submitted,

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Enclosure: Petition for Extension of Time (two months)

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